AMENDMENTS TO THE CLAIMS

In accordance with 37 C.F.R. §1.121, a claim listing including the status and text of all claims as currently presented appears below.

1. (Currently amended) A method of making a multi-layer electronic component, comprising the steps of:

providing a plurality of dielectric layers;

providing a plurality of conductive tabs spirally aligned and interspersed among said plurality of dielectric layers**, said plurality of conductive tabs respectively configured such that at least a portion thereof is exposed**; and

plating a layer of termination material on **the exposed portions of** said conductive tabs whereby said plurality of tabs are connected together.

2. (Original) A method as in claim 1, wherein the step of providing a plurality of conductive tabs comprises printing individual layers of conductive material at selected locations on selected surfaces of selected dielectric layers.

3. (Original) A method as in claim 1, further comprising the step of:

exposing portions of the plurality of conductive tabs by opening a via through the plurality of dielectric layers prior to the step of plating.

4. (Original) A method as in claim 1, wherein said step of plating comprises exposing said conductive tabs to an electroless copper solution.

5. (Currently amended) A method of directing the formation of plating material in a multi-layer electronic component, comprising the steps of:

embedding a plurality of conductive tabs at selected locations in a plurality of layers of dielectric material**, wherein said plurality of conductive tabs are respectively positioned at selected edges of said plurality of dielectric layers**; and

exposing the plurality of conductive tabs to a plating solution whereby the embedded conductive tabs form nucleation points for plating material within the plating solution and guide the direction of the deposition of the plating material along the exposed plurality of conductive tabs.

6. (Original) The method of claim 5, wherein the surface area and positioning of the exposed conductive tabs is varied whereby the surface area and geometry of the plating material is controlled.

7. (Currently amended) The method of claim 6, wherein the surface area and positioning of the exposed conductive tabs is varied such that the surface area of the plating material is formed into a ~~generally~~**substantially** planar discoidal formation.

8. (Currently amended) The method of claim 7, wherein the ~~generally~~**substantially** discoidal formation of plating material is configured as ball limiting metallurgy.

9. (Currently amended) The method of claim 6, wherein the surface area and positioning of the exposed conductive tabs is varied such that the surface area of the plating material is formed into a ~~generally~~**substantially** linear spiral formation.

10. (Currently amended)The method of claim 9, wherein the ~~generally~~**substantially** linear spiral formation is configured as an inductive element.

11. (Original) A method of making a multi-layer electronic component, comprising the steps of:

providing a plurality of insulating substrates each having an upper and a lower surface, said substrates each being delimited laterally by edges;

interleaving a plurality of electrodes between selected of said plurality of insulating substrates;

exposing varied width portions of said electrodes along at least one edge of said plurality of substrates; and

plating at least one layer of termination material on the exposed portions of said electrodes.

12. (Original) The method of claim 11, further comprising the step of continuing the plating process until the exposed portions of said electrodes are connected.

13. (Original) The method of claim 11, wherein the step of plating is performed using an electroless process followed by an electrochemical process.

14. (Original) The method of claim 11, wherein the step of plating is performed using an electroless process.

15. (Original) The method of claim 14, wherein the electroless process comprises submersing the multi-layer electronic component in an electroless copper plating solution to form a copper termination layer.

16. (Original) The method of claim 15, further comprising the step of covering the copper termination layer with a resistive layer.

17. (Original) The method of claim 16, further comprising the step of plating the resistive layer with a conductive layer.

18. (Original) The method of claim 11, wherein the step of exposing comprises:

providing the electrodes with non-uniformly cross-sectioned tab portions;

positioning the electrodes at laterally displaced locations among said dielectric layers; and

cleaving edges of the interleaved electrodes and dielectric layers whereby varied width portions of the tab portions of the electrodes are exposed.

19. (Original) The method of claim 18, wherein said providing step comprises providing the electrodes with rounded tab portions.